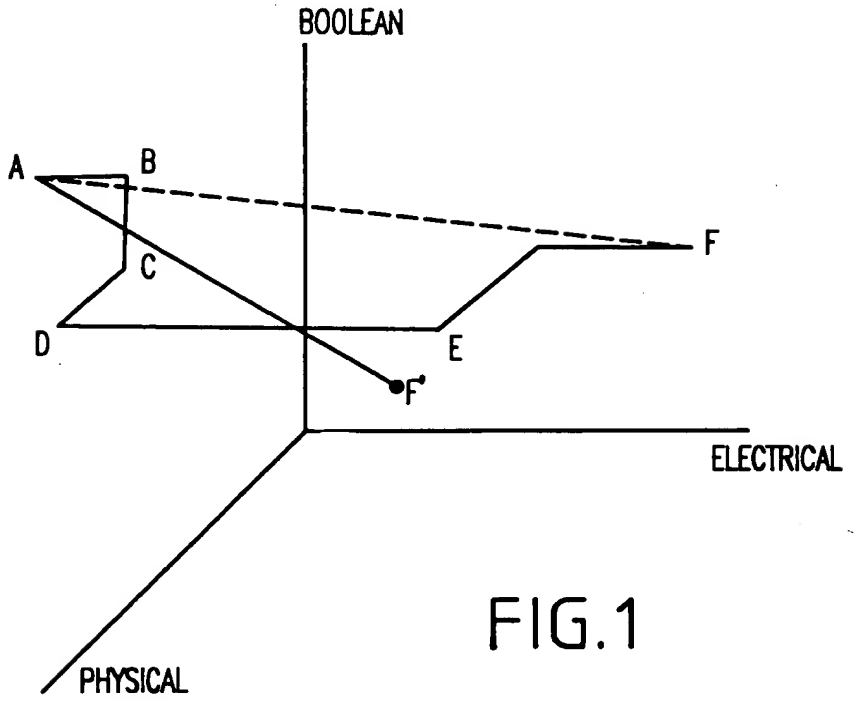
BOOLEAN
A
B
C
D
E
F
F'
ELECTRICAL
PHYSICAL

FIG.1

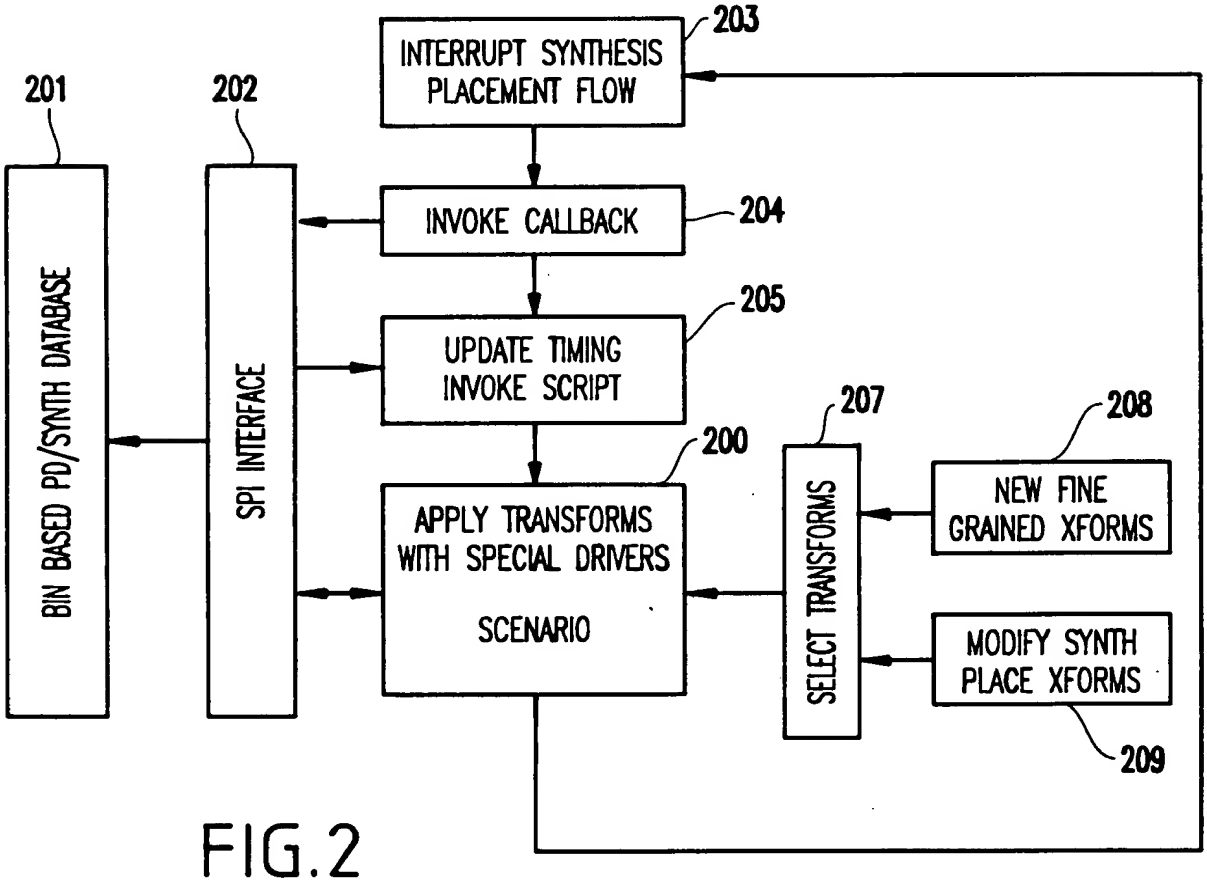
201
202
203
INTERRUPT SYNTHESIS PLACEMENT FLOW
INVOKE CALLBACK
204
UPDATE TIMING INVOKE SCRIPT
205
BIN BASED PD/SYNTH DATABASE
SPI INTERFACE
APPLY TRANSFORMS WITH SPECIAL DRIVERS
SCENARIO
200
207
SELECT TRANSFORMS
208
NEW FINE GRAINED XFORMS
MODIFY SYNTH PLACE XFORMS
209

FIG.2

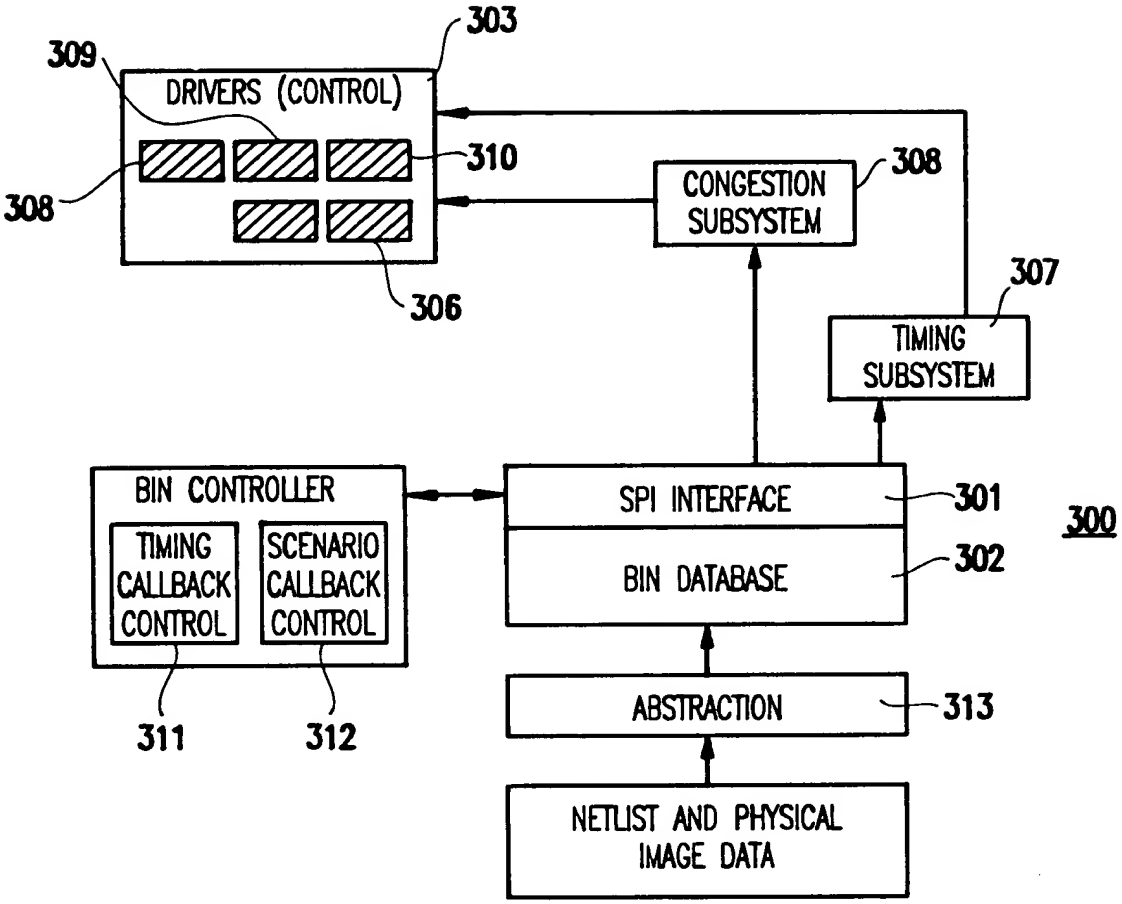
303
309
DRIVERS (CONTROL)
310
308
308
CONGESTION SUBSYSTEM
306
307
TIMING SUBSYSTEM
BIN CONTROLLER
TIMING CALLBACK CONTROL
SCENARIO CALLBACK CONTROL
311
312
SPI INTERFACE
301
300
BIN DATABASE
302
ABSTRACTION
313
NETLIST AND PHYSICAL IMAGE DATA

FIG.3

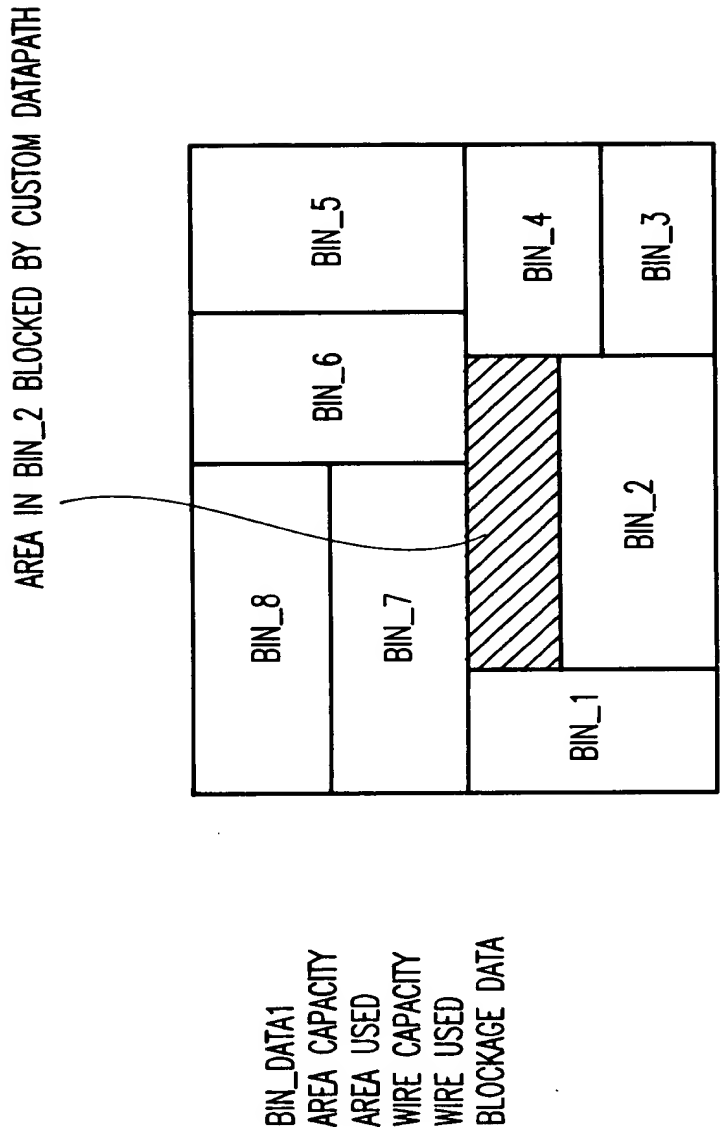
AREA IN BIN_2 BLOCKED BY CUSTOM DATAPATH
BIN_5
BIN_4
BIN_3
BIN_6
BIN_8
BIN_7
BIN_2
BIN_1
BIN_DATA1
AREA CAPACITY
AREA USED
WIRE CAPACITY
WIRE USED
BLOCKAGE DATA

FIG.4

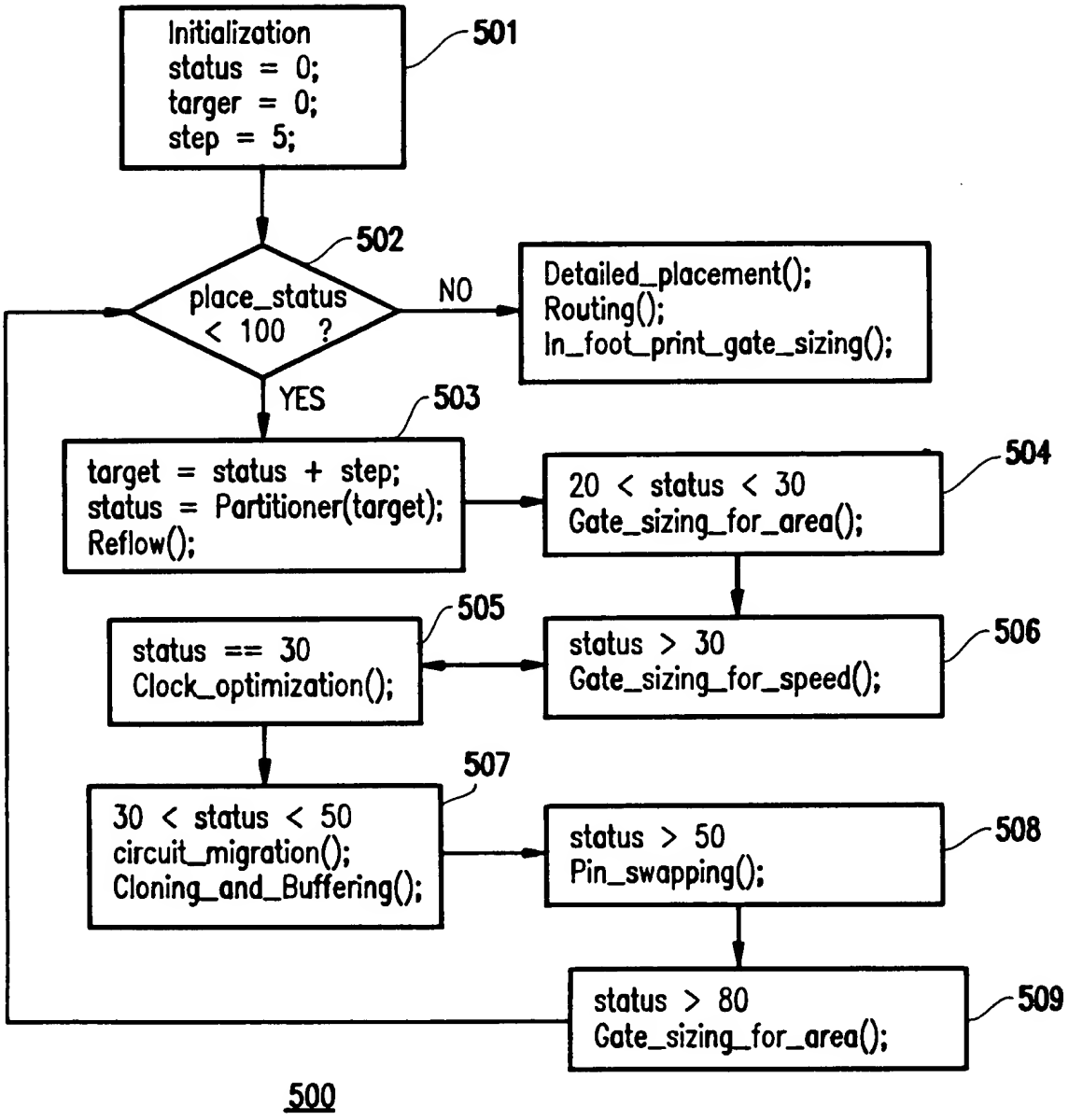
Initialization
status = 0;
targer = 0;
step = 5;
501
502
place_status
< 100 ?
NO
Detailed_placement();
Routing();
In_foot_print_gate_sizing();
YES
503
target = status + step;
status = Partitioner(target);
Reflow();
20 < status < 30
Gate_sizing_for_area();
504
status == 30
Clock_optimization();
505
status > 30
Gate_sizing_for_speed();
506
507
30 < status < 50
circuit_migration();
Cloning_and_Buffering();
status > 50
Pin_swapping();
508
status > 80
Gate_sizing_for_area();
509
500

FIG.5

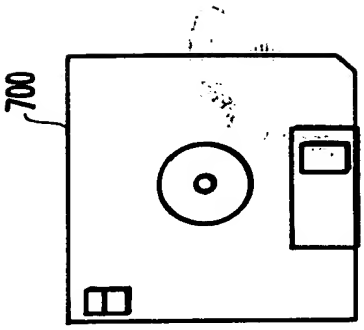
700

FIG.7

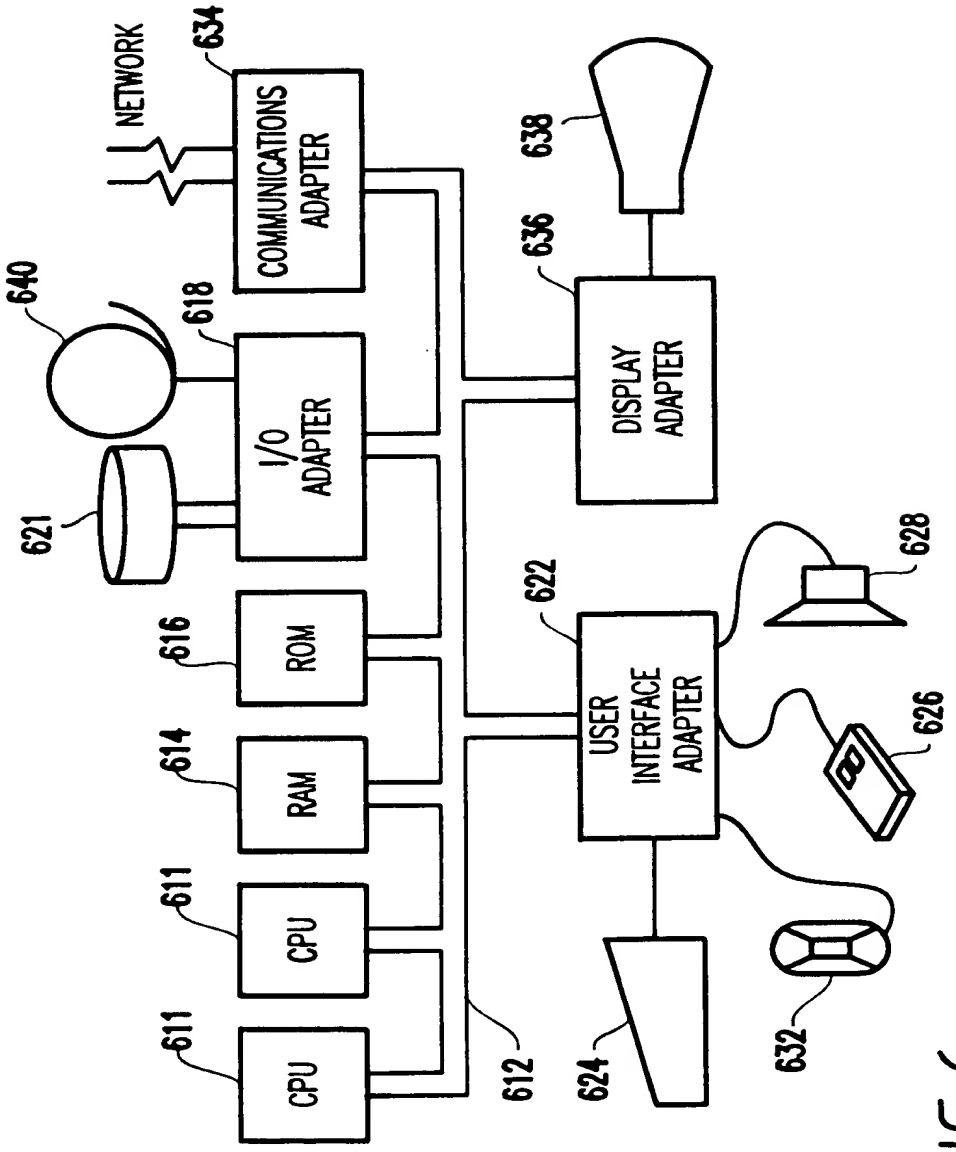
NETWORK
634
COMMUNICATIONS ADAPTER
638
636
DISPLAY ADAPTER
640
618
I/O ADAPTER
621
616
ROM
614
RAM
611
CPU
611
CPU
612
622
USER INTERFACE ADAPTER
628
626
624
632

FIG.6